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#### **CLAIMS**

What is claimed is:

- A method of fabricating a first halo region and a second halo region for a circuit device of a first conductivity type and having a gate structure with first and second sidewalls, comprising:
  - forming the first halo region of a second conductivity type by implanting the substrate with impurities in a first direction toward the first sidewall of the gate structure;
  - forming the second halo region of the second conductivity type by implanting the substrate with impurities in a second direction toward the second sidewall of the gate structure; and
  - wherein the first and second halo regions are formed without implanting impurities in a direction substantially perpendicular to the first and second directions.
- 15 2. The method of claim 1, wherein the first conductivity type comprises p-type and the second conductivity type comprises n-type.
  - 3. The method of claim 1, wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type.
  - 4. The method of claim 1, wherein the first direction is substantially perpendicular to the first sidewall.
- 5. The method of claim 1, wherein the first direction is substantially perpendicular to the first sidewall and the second direction is substantially perpendicular to the second sidewall.
  - 6. The method of claim 1, wherein the implanting impurities in the first direction is performed at an angle of about 15 to 45° from vertical.

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- 7. The method of claim 6, wherein the implanting impurities in the second direction is performed at an angle of about 15 to 45° from vertical.
- 8. A method of fabricating halo regions for a first group of transistors on a substrate substantially aligned with a first axis and a second group of transistors on the substrate substantially aligned with a second axis that is substantially perpendicular to the first axis, comprising:
  - forming halo regions for the first group of transistors by implanting the substrate with impurities in a first direction substantially perpendicular to the first axis, and implanting the substrate with impurities in a second direction substantially opposite the first direction and substantially perpendicular to the first axis, and without implanting impurities in a direction substantially parallel to the first axis; and
  - forming halo regions for the second group of transistors by implanting the substrate with impurities in a third direction substantially perpendicular to the second axis, and implanting the substrate with impurities in a fourth direction substantially opposite the third direction and substantially perpendicular to the second axis, and without implanting impurities in a direction substantially parallel to the second axis.
- 9. The method of claim 8, wherein the first and second groups of transistors comprise nchannel transistors.
- The method of claim 8, wherein the first group of transistors have a first conductivity type and the second group of transistors comprises a second conductivity type.
  - 11. The method of claim 10, comprising masking one of the first and second groups of transistors while implanting the other of the first and second groups of transistors.

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- 12. The method of claim 8, wherein the implanting impurities in the first and second directions is performed at an angle of about 15 to 45° from vertical.
- 13. The method of claim 8, wherein the implanting impurities in the third and fourth directions is performed at an angle of about 15 to 45° from vertical.
  - 14. A method of fabricating first and second halo regions for a n-channel transistor having a first gate structure and third and fourth halo regions for a p-channel transistor having a second gate structure, comprising:

masking the p-channel transistor;

forming the first halo region extending beneath the first gate structure by implanting impurities in a first direction toward a first sidewall of the first gate structure;

forming the second halo region extending beneath the first gate structure by implanting impurities in a second direction substantially opposite to the first direction toward a second sidewall of the first gate structure;

unmasking the p-channel transistor and masking the n-channel transistor;

forming the third halo region by implanting impurities in the first direction toward a first sidewall of the second gate structure;

forming the fourth halo region by implanting impurities in the second direction toward a second sidewall of the second gate structure; and

wherein the first, second, third and fourth halo regions are formed without implanting impurities in a direction substantially perpendicular to the first and second directions.

- The method of claim 14, wherein the implanting of impurities in the first and second directions is performed at an angle of about 15 to 45° from vertical.
  - 16. The method of claim 14, wherein the impurities of the first and second halo regions comprise boron, BF<sub>2</sub> or indium.

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- 17. The method of claim 14, wherein the impurities of the third and fourth halo regions comprise phosphorus, arsenic or antimony.
- 18. A method of manufacturing, comprising:
  - forming first and second halo regions for each of a first group of n-channel transistors aligned along a first axis by implanting impurities beneath gate structures of each of the first group of n-channel transistors from first and second substantially opposite directions toward opposite sides of the gate structures of the first group of n-channel transistors;
  - forming third and fourth halo regions for each of a second group of n-channel transistors aligned along a second axis substantially perpendicular to the first axis by implanting impurities beneath gate structures of each of the second group of n-channel transistors from third and fourth substantially opposite directions toward opposite sides of the gate structures of the second group of n-channel transistors;
  - forming first and second halo regions for each of a first group of p-channel transistors aligned along the first axis by implanting impurities beneath gate structures of each of the first group of p-channel transistors from first and second substantially opposite directions toward opposite sides of the gate structures of the first group of p-channel transistors;
  - forming third and fourth halo regions for each of a second group of p-channel transistors aligned along the second axis by implanting impurities beneath gate structures of each of the second group of p-channel transistors from third and fourth substantially opposite directions toward opposite sides of the gate structures of the second group of p-channel transistors; and
  - wherein the first and second halo regions of the first group of n-channel transistors and the first group of p-channel transistors are formed without implanting impurities in a direction substantially perpendicular to the first and second directions, and the third and fourth halo regions of the second group of n-channel transistors and the second group of p-channel transistors are formed

without implanting impurities in a direction substantially perpendicular to the third and fourth directions.

- 19. The method of claim 18, wherein the implanting of impurities in the first, second, third and fourth directions is performed at an angle of about 15 to 45° from vertical.
  - 20. The method of claim 18, wherein the impurities of the comprise boron, BF<sub>2</sub> or indium.
- The method of claim 18, wherein the impurities of the first, second, third and fourth halo regions of the first and second groups of p-channel transistors comprise phosphorus, arsenic or antimony.

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